



PCBA Design for Six Sigma Project presented to the Boulder Chapter ASQ

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DC Main Brick DFX Optimization

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Master Black Belt: Paul VonLoh

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Problem Statement & Business Case:

Due to the complexity of the DC Main Brick Printed Circuit Board Assembly (PCBA), AE determined the need for design, cost and quality optimization. Six Sigma tools will be used to define, measure and analyze the options. Once the potential solutions are defined, a design review of up to three PCBA technologies for the DC Main Brick will be used to obtain the best quality, price and delivery. The technologies under review will be Surface Mount (SMT), Pin Thru Hole (PTH) and Press Fit. Each technology has quality, cost and reliability advantages and disadvantages.

Objective Statement:

This project is intended to *decrease cost by at least \$XX.XX* for each assembly of the PCBA, effective 1/07/2011, as measured by the Bill of Material for the PCBA parts cost.

Conclusions, Recommendations, & Business Results

After numerous design reviews and PFMEA discussions it was decided that the best overall design uses a combination of Surface Mount (SMT) and Pin Thru Hole Technology. Press Fit was determined to have assembly advantages, but the cost and reliability implications outweighed the advantages. The optimization resulted in a savings of \$XXX.XX per PCBA. Annual usage of XXXX equates to \$X,XXX,XXX.00 per year.

A savings of US \$X,XXX,XXX.00 in 2011



Definition

Problem Statement: Due to the complexity of the DC Main Brick Printed Circuit Board Assembly (PCBA), AE determined the need for design, cost and quality optimization. Six Sigma tools will be used to define, measure and analyze the options. Once the potential solutions are defined, a design review of up to three PCBA technologies for the DC Main Brick will be used to obtain the best quality, price and delivery. The technologies under review will be Surface Mount (SMT), Pin Thru Hole (PTH) and Press Fit. Each technology has quality, cost and reliability advantages and disadvantages.

Goal(s): This project is intended to decrease cost by at least \$XX.XX for each assembly of the PCBA, effective 1/07/2011, as measured by the Bill of Material for the PCBA parts cost.

Project Scope:

Paramount VHF RF Power Delivery System
 Scope: DC Main Brick PCBA design used in the Paramount VHF

Business Case

Direct Savings or Revenue: The project intended to decrease cost by at least \$XX.XX for each assembly of the PCBA. The cost will be measured by the DC Main Brick PCBA Part Number 33020100 Bill of Material. The project resulted in a savings of \$XXX.XX per PCBA. Annual usage of XXXX equates to a savings of \$X,XXX,XXX.00 per year.

Indirect Savings: The plan is to have indirect process, quality and reliability savings.

Team

<u>Name, Title</u>	<u>Team Function</u>
Eddie Khong, Master Black Belt, AESZ	Champion
Brian Svoboda, Black Belt	Exec. Champion
Paul VonLoh	MBB
Byron Murray, NPI PCBA SQE	Green Belt
John Dorrenbacher, Design EE	Process Owner
Michael Broccardo, Mfg. Eng.	Manufacturing
Chad Burnett, MPM	Materials
EG Ooi, Plexus Penang	Supplier SME
Salim Merchant, Plexus San Jose	Supplier SME

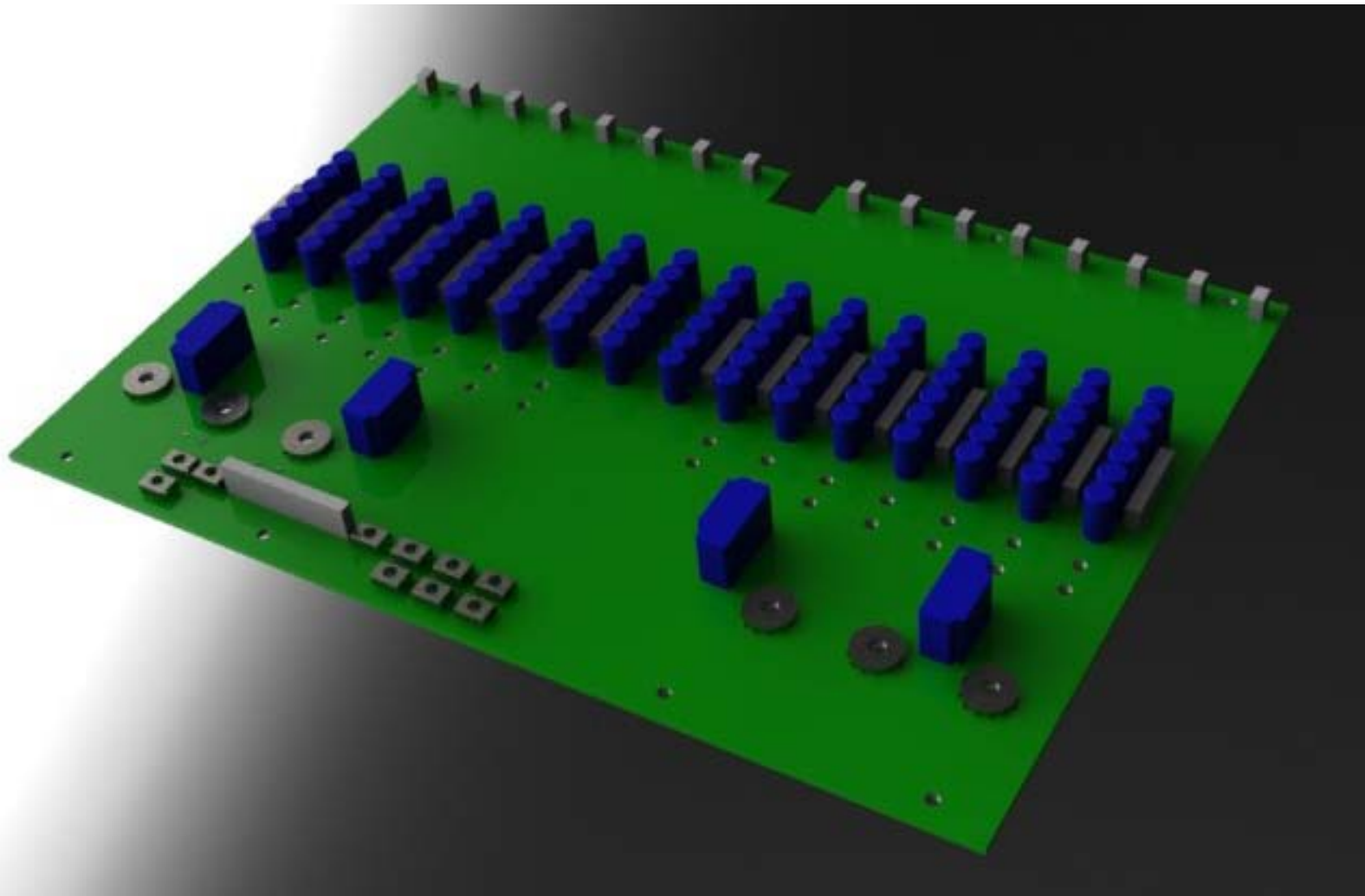
Schedule

<u>Tollgate</u>	<u>Scheduled</u>	<u>Complete</u>
Charter:**	8/27/2010	8/27/2010
Define:	9/17/2010	9/17/2010
Measure	9/24/2010	9/24/2010
Analyze:	10/1/2010	10/1/2010
Improve:	10/8/2010	10/8/2010
Control:	10/8/2010	10/8/2010
Certification	10/13/2010	10/15/2010

** Note: GBs are encouraged to tollgate their Charter with their champion



Define Phase
Conceptual Picture of the DC Main Brick PCBA



The DC Brick Main is 11"X16"X.125" with 4oz copper and weighs ~8lbs when the daughter cards (Bricks) are installed.



In the Define Phase we isolated the scope to optimizing the DC Main Brick Printed Circuit Board Assembly for quality, price and delivery. In the Measure Phase (and or Identify Phase - DFSS) we plan to look at the factors that influence quality, price and delivery.

This project was performed in the design world of AE and hence follows more closely the DFSS methodology (D-IDOV). However this presentation was prepared in line with the DMAIC training, but I attempted to match the phases for both methodologies.



Measure Phase
IPO

OUTPUTS

INPUTS

PROCESS

Material Cost

Material Availability

Process Cost

Process Flow

PCBA Design

Quality

Cost

Supply Chain

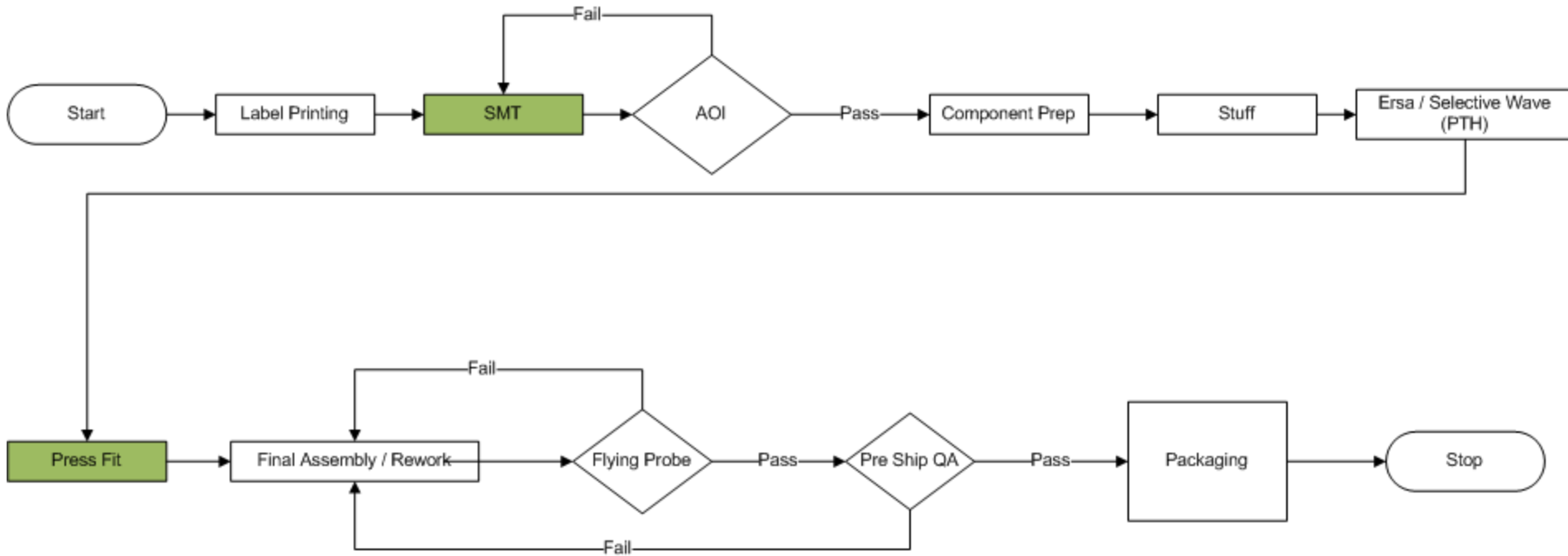
Reliability

Supplier Capability

All designs have advantages and disadvantages.



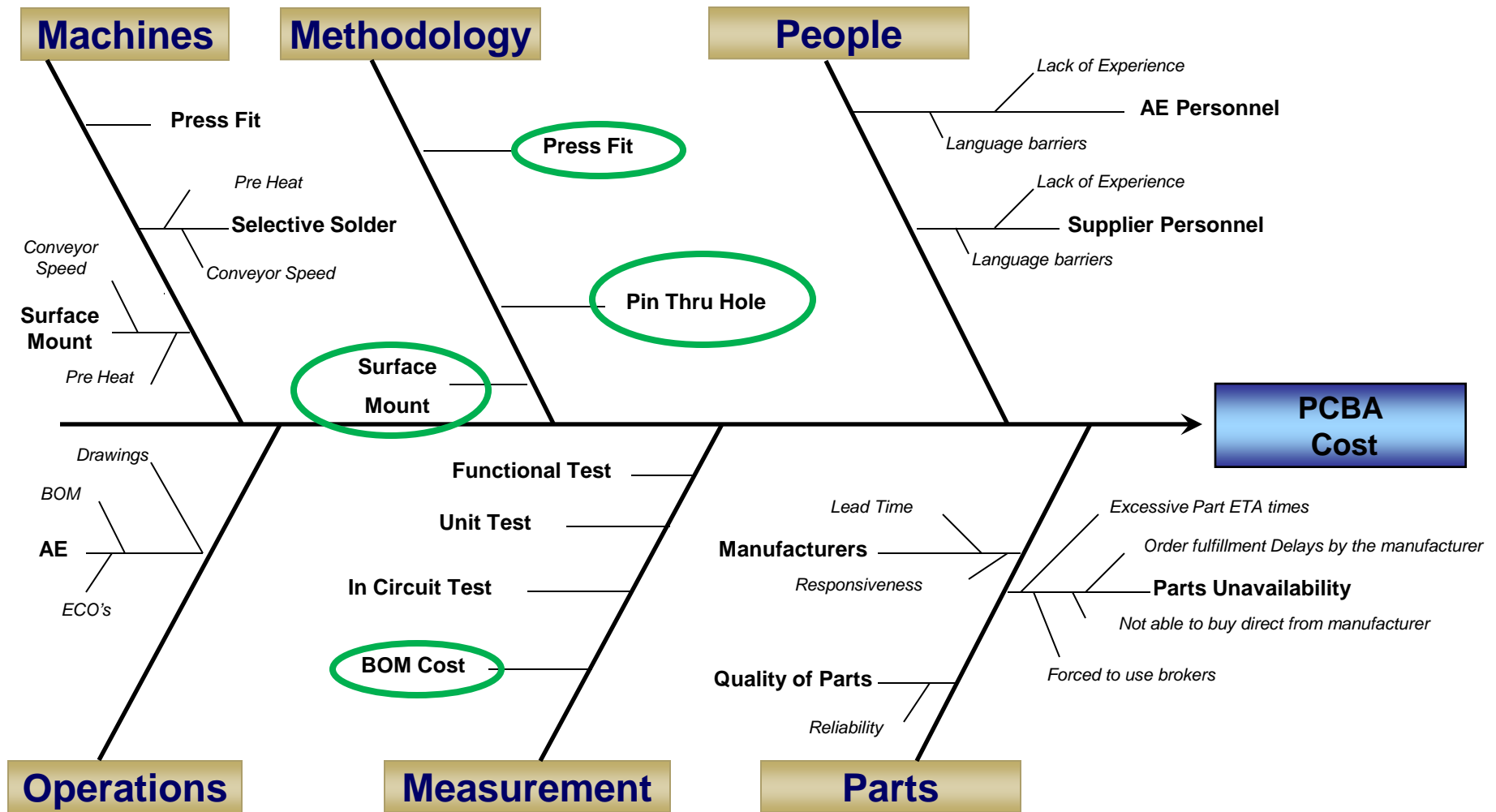
Measure Phase PCBA Process Flow Chart



Note: The green boxes identify the optional processes.



Measure Phase Cause and Effect (Fishbone) Diagram



Surface Mount, Pin Thru Hole and Press Fit have the most impact on PCBA cost.



In the Measure Phase (and or Identify Phase - DFSS) we looked at the factors that influence quality, price and delivery. The primary factors that influence quality, price and delivery are the types of components used on the PCBA. The technologies under review in the Analyze Phase (and or Design Phase - DFSS) will be Surface Mount (SMT), Pin Thru Hole (PTH) and Press Fit. Each technology has quality, cost and reliability advantages and disadvantages.



PCBA Process A:

SMT -Selective Wave

This process would utilize SMT connectors that interconnect to 16 Bricks (daughter PCBA's) and the small capacitors and resistors would be SMT. The selective wave would be used for the large capacitors and other PTH components.

PCBA Process B:

SMT-Selective Wave – Press Fit

This process would utilize Press Fit connectors that interconnect to 16 Bricks and the small capacitors and resistors would be SMT. The selective wave would be used for the large capacitors and other PTH components.

PCBA Process C:

Selective Wave

This process would utilize PTH connectors that interconnect to 16 Bricks and the small capacitors and resistors would be PTH.



COMMENT ON PROCESS A: Of the three solutions this solution will provide the most reliable & ease of manufacturing. The SMT connectors are preferred to through hole connectors specifically due to thickness of the board. The solder fillet in these holes will be difficult even using ERSA selective wave and/or wave solder machine. The wave solder machine has higher probability of 'insufficient' solder in the fillets.

COMMENT ON PROCESS B: The process will be slightly different than stated above. In place of performing operation of press fit, we would have Ersa Selective wave or wave solder operation prior to press fit. One issue is that RoHS connectors are difficult to press fit due to tolerance issues of the pin & PCB hole. Normally the PCB press fit hole tolerance has to be +/- .002" as compared to normal of +/- .003"



COMMENT ON PROCESS C: Strictly from process point of view the difference between Ersas Selective wave & wave solder operation is that with Ersas Selective wave a more complete solder fillet can be achieved in the hole compared to wave solder machine. And as the thickness of the board increases this issue becomes more critical because achieving a high percentage of hole fillet with wave solder becomes difficult.



In the Analyze Phase (and or Design Phase - DFSS) Surface Mount (SMT), Pin Thru Hole (PTH) and Press Fit were evaluated, and we learned that having a PCBA using mixed technology was the best overall solution. In the Improve Phase (and or Optimize Phase - DFSS) we plan to use multiple six sigma tools to narrow the focus and optimize the design.



Improve Phase Design Failure Modes Effects Analysis (DFMEA)

DESIGN FAILURE MODE EFFECTS AND CRITICALITY ANALYSIS (DFMEA) WORKSHEET

DFMECA Team: M. Shover
 Assy/Product Name: Paramount VHF 6060
 Assy/Product Number & Rev: DC brick main
 Analyst: M. Shover

Initial DFMECA Data					Detailed DFMECA Data					
ID Number	Function Description	System Operating Mode	Functional Failure Mode	Severity Class	Components Causing Failure Mode	Failure Mode of Component	Potential Design Control	Prob. Of Failure Mode	Likelihood of Comp Failure	Prob x Likelihood of Comp Failure
1	Energy storage for bricks		At lease one brick output at zero voltage	II	C47	short		0.53	1.4	0.742
					C48	short		0.53	1.4	0.742
					C49	short		0.53	1.4	0.742
					C50	short		0.53	1.4	0.742
					C51	short		0.53	1.4	0.742
					C52	short		0.53	1.4	0.742
					C35	short		0.53	1.4	0.742
					C36	short		0.53	1.4	0.742
					C37	short		0.53	1.4	0.742
					C38	short		0.53	1.4	0.742
					C39	short		0.53	1.4	0.742



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Note from Michael Shover: “The analysis is attached. Not much to discuss, as the board is essentially a backplane with storage caps and current sensors. The only items of moderate criticality are the current sensors, but we have lots of experience using these exact parts. All the capacitors are sufficiently derated. I don’t anticipate problems with this board.”



Improve Phase Process Failure Modes Effects Analysis (PFMEA)

Assembly Revision:	FMEA start date: 9/1/2010
Type: <input type="checkbox"/> DESIGN <input checked="" type="checkbox"/> PROCESS	FMEA due date: 10/8/2010

Team Members:

Step # or sort string	Process Function / Operation	Potential Failure Mode	Effects of Failure	Potential Cause of Failure	Control	SEV	OCC	DET	RPN	CRIT	
									0	0	
	23020079 PCB 6060 NEW VHF DC MAIN #1	Open Trace	Fails Field	Design	Design Rules	7	5	4	140	35	
				Fabrication	Test				0	0	
	18020009-00 IC CURRENT SENSOR LAH	Open Solder	Fails Field	Machine Profile	Rev Ctrl Machine FW	9	6	9	486	54	
	18020009-00.jpg			Machine Set up	Operator check list				0	0	
				Component Contamination	Operator gloves				0	0	
					PCBA Design Layout	Design Rules	3	6	3	54	18
		Solder Short	Fails ICT Test		Machine Profile	Rev Ctrl Machine FW	3	6	3	54	18
				Machine Set up	Operator check list				0	0	
		Component backwards	Not able to insert into PCB			7	1	1	7	7	
		Component defective - Component has active devices inside the component including an Asic.	Fails Unit Test	Defective from supplier	Supplier Test	7	5	4	140	35	
			Fails Field	Operator Handling	ESD Handling Procedure				0	0	
									0	0	



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Improve Phase Design Evaluation Matrix

Evaluation Perspectives	Design Process A	Design Process B	Design Process C
Quality	+	-	S
Cost	+	-	-
Supply Chain	+	-	-
Supplier Capability	S	S	S
Manufacturability	+	-	+
Complexity	S	+	S
Performance	S	S	-
Reliability	S	S	-
Robustness	-	+	+
# of +'s	4	2	2
# of -'s	1	4	4
# of S's S=Same	4	3	3



Financial Benefit: Cost Comparison between PTH, SMT, and Press Fit

AE Part Number	Description	Qty	Process B		Process A	
			PTH Comp Cost	PTH EXT Cost EAU 2500	SMT Comp Cost	SMT EXT Cost EAU2500
92270010	CAP 2.2UF CM 100V 10% X7R 1210	24				
95070002	DIODE 12V0 BD ESD PROTECTION SOD323	4				
91020060	RES 20K THF 1/8W .1% 0805	8				
92220048	TR CAP CER X7R 1U0 10% 50V 0805	4				

By using the above Surface Mount (SMT) components we are able to save \$XX,XXX.00 per year versus using Pin Thru Hole (PTH) components.

AE Part Number	Description	Qty	Process B		Process C	
			PTH Comp Cost	PTH EXT Cost EAU 2500	SMT Comp Cost	SMT EXT Cost EAU2500
21500802-Z02	100 AMP POWER TAP PARAMOUNT VHF	6				

By using the above Pin Thru Hole (PTH) component we are able to save \$X,XXX,XXX.00 per year versus using the Press Fit component.

\$XX,XXX + \$X,XXX,XXX equates to a savings of \$X,XXX,XXX.00 per year



In the Improve Phase (and or Optimize Phase - DFSS) we used multiple six sigma tools to narrow the focus and optimize the design. The final design used mixed technology utilizing the best overall cost, quality and delivery resulting in an annual savings of \$X,XXX,XXX.00. In the Control Phase (and or Verify Phase - DFSS) we outline how the design is controlled.



Advanced Energy controls the design through the Engineering Change Order Process. The following PCBA documents are ECO controlled. (Examples are provided in the Appendix)

- 1. Bill of Material (BOM)***
- 2. PCB Drawing***
- 3. Schematic***
- 4. Source Control Drawing (SCD)***
- 5. Supplier Process Matrix (SPM)***
- 6. PCBA Test Specification***



Control Phase PFMEA Actions

QF0445AD - REVISED MAY 13, 2009

Prepared By: Byron Murray							
FMEA Number:							
Reason for FMEA: Design Review							
Analysis & Recommended Corrective Actions	Owner	Due date	SEV	OCC	DET	RPN	Comments
						0	
						0	
PTH hole size to be optimized for next build.						0	
Solder Short - Need to ensure solder does not reach center hole. Need to include note in SCD.						0	
						0	
Part Lifting - Need to ensure Plexus develops a fixture to hold part flat						0	

Actions from the PFMEA will be documented in the BOM, PCB Drawing, Schematic, Source Control Drawing (SCD), Supplier Process Matrix, or PCBA Test Specification.



Due to the complexity of the DC Main Brick Printed Circuit Board Assembly (PCBA), AE determined the need for design, cost and quality optimization. Six Sigma tools were used to define, measure and analyze the options. The final design uses mixed technology utilizing the best overall cost, quality and delivery resulting in an annual savings of \$X,XXX,XXX.00.

The most valuable tool in this project was collaboration of the PFMEA. The PFMEA generated communication between the designer and the supplier that might not have happened otherwise.



Appendix

Part 9: APPENDIX (Optional)

Include additional data, charts, figures, tables, etc. not included in other parts of the report



PCBA Bill of Material (BOM)

Cust PN	Description	Qty
23020079	PCB 6060 NEW VHF DC MAIN #1 @A	1
21500802-Z02	100 AMP POWER TAP PARAMOUNT VHF	6
18020009-00	IC CURRENT SENSOR LAH	4
12610012	CAP 560UF EC 35V ESR18 10X25 0R500	96
90120021	HDR 32M ST HDR PC DRW 100 SMT	16
90020019	HDR 6 PIN	16
14500029	TBLK 01P 40A0 00V0 PC M4 T/S 10-PIN	8
92270010	CAP 2.2UF CM 100V 10% X7R 1210	24
90120017	CON 012M ST HDR PC 630 STK DRW 100 SMT	2
95070002	DIODE 12V0 BD ESD PROTECTION SOD323	4
91020060	RES 20K THF 1/8W .1% 0805	8
92220048	TR CAP CER X7R 1U0 10% 50V 0805 @A	4

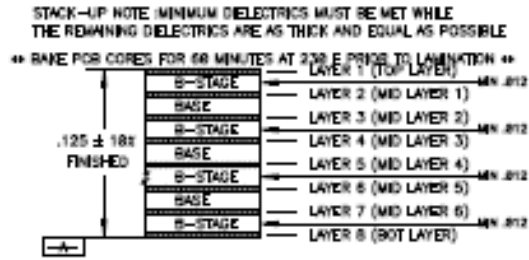


Microsoft Office
Excel Worksheet





- ◆ - QUANTITY INCLUDES DATUMS 'B' & 'C'.
- ◆◆ - .061 PLATED SLOTS
- ◆◆◆ - .042 PLATED SLOTS



DETAIL A
SCALE: NONE

NOTE: THIS PART IS DESIGNED FOR HIGH VOLTAGE APPLICATIONS AND MEETS SPECIFIC SAFETY STANDARDS. DO NOT PERMANENTLY APPLY WITHIN THE FINISHED BOARD OUTLINE ANY THEIVING PATTERNS, VENTING PATTERNS, CONDUCTIVE INKS OR ANY OTHER CONDUCTIVE MATERIALS WITHOUT PRIOR WRITTEN AUTHORIZATION FROM THE PCB DESIGN AND REGULATORY COMPLIANCE ENGINEERING GROUPS OF ADVANCED ENERGY INDUSTRIES INC.

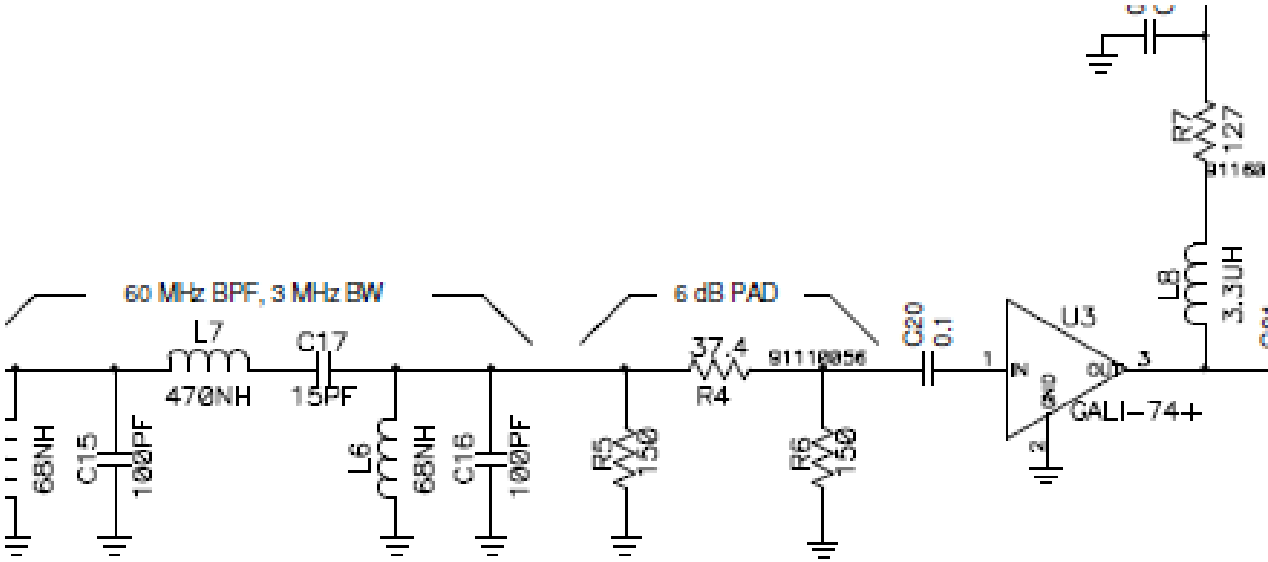
NOTE: ANY DEVIATION FROM THE SPECIFICATIONS ON THIS DRAWING MUST HAVE PRIOR WRITTEN APPROVAL.



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Sample Schematic



Control Phase Supplier Process Matrix



Supplier Process Matrix

Supplier :	Plexus manufacturing Sdn. Bhd		Facility/Location :	Plexus, Penang	
AE SQE :	Eddie Khong, Don Lim, Andy Wu and Alfred Hou	Date : 12 Jan 2010	Supplier's Quality Manager :	CC Chan	Rev Date : 12 Jan 2010

Manufacturing Process Matrix

Step	Process	Mfg. Equipment, Fixture, Tools	Consumables	Feature Creation Controls	Verification/Validation Methods	Reference Specification and Supplier Document	Out-of-control reaction
00	Material Ordering	AE AVL	N/A	JDE system	N/A	AE AVL	Contact supplier
10	Material Receipt	Labels Printer	Labels	Invoice Packing List JDE system	Check part number against AVL.	AVL	Quarantine part and inform Product Engineer/Supervisor.
20	IQA	Caliper Pin Gauge Microscope (Olympus) Mitutoyo Microscope	3M Transparent Tape 600	IPC-A-600 Part Receiving Checklist (682F230) Part Inspection Instruction (682F244)	Checklist	IPC-A-600 AVL AE Drawings	Quarantine part and inform Product SQE and IQA Enginner/Supervisor. Non Conforming Material



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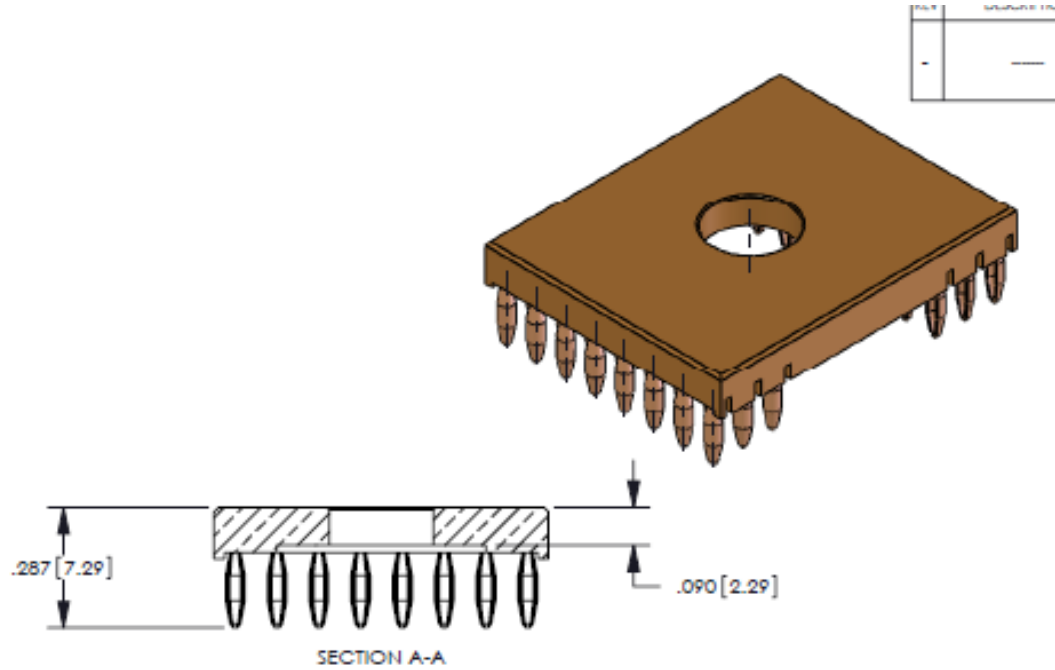
5	PCBA INFORMATION	4
5.1	PCBA Dimensions:	4
5.2	PCBA Node Count / Access Count:	4
5.3	Critical Components:	4
5.4	Other Information:	4
6	INSPECTION	4
6.1	Inspection Criteria	4
6.2	Automated Optical Inspection (AOI)	4
6.3	X-ray (AXI)	4
6.4	Poka-Yoke	4
6.5	Manual Inspection	5
7	ELECTRICAL TEST SPECIFICATION	5
7.1	Flying probe testing	5
7.2	ICT 3070 testing	5
7.3	Chip programming	5
7.4	Functional Test	6
7	FUNCTIONAL TEST DETAIL	6
8	PACKAGING	6
8.1	Instructions	6
APPENDIX A		6



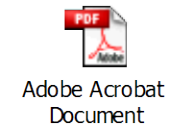
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Word Document



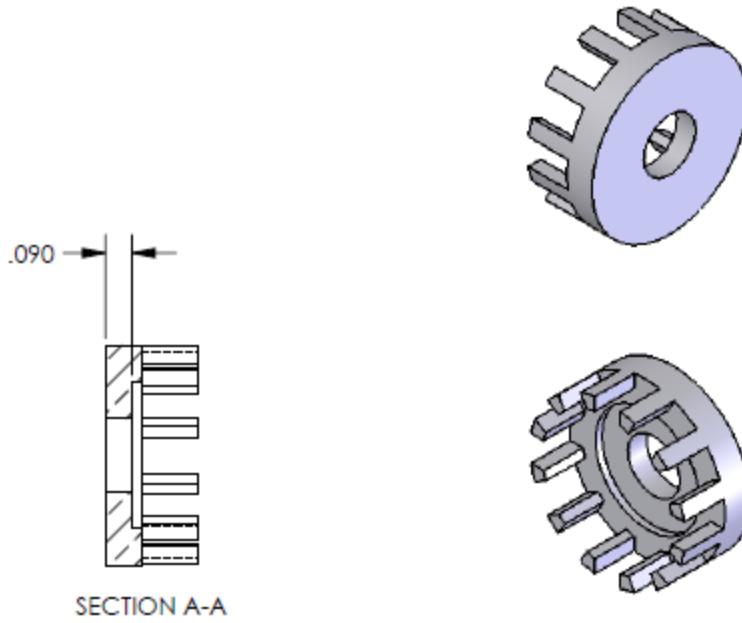
Winchester Power Tap Press Fit Design



Note: \$XX per part



AE Power Tap Pin Thru Hole Design



Note: \$X.X per part



Adobe Acrobat
Document



PCBA Design for Manufacturability Review

Plexus DFM Review

Customer:	Advanced Energy
Assembly #:	33020071
Rev:	A
Assembly Name:	PCBA 6060 NEW YHF DC MAIN

Issue Number	Date Reviewed	DFM type	Reviewed By	Severity Level*	DFM Guidelines Section #	DFM Guidance, Issue Description/Location(s)
Component Selection - Bill of Materials (BOM)						
		Post-Asy		General	102.3.3	Rework Wires should be avoided.
1	23-Jul-10	Post-Asy	Mike Rifahi	Minor	102.3.5	SMT components should be selected to PTH hole components
		Post-Asy		Minor	102.3.6	Number of components per assembly should be minimized . i.e.- chip array vs. individual chips
		Post-Asy		Minor	102.3.7	Number of component part numbers should be minimize. i.e.- combined tolerances, voltages, packages
		Post-Asy		Minor	102.6.4	PTH Lead protrusion should be at least .020" for lead visibility
		Post-Asy		General	102.6.4	PTH components spec'd out so lead protrusion is less that .070" to eliminate clipping.
		Post-Asy		Minor	RoHS	All parts on BOM required to be RoHS compliant in order to comply.
		Post-Asy		Moderate	RoHS	Recommend not utilizing PB-Free BGA package in a non-RoHS or leaded process. Assembly requires reballing package.
Padstack / PCB Land Pattern						
		Post-Asy		Moderate	103	Land Pattern Design.
		Post-Asy		Minor	103.14.3	Polarization Indicators for Polarized Components in Silk screen.



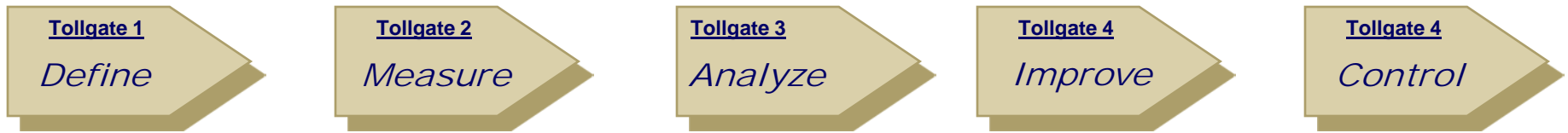
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➔ = required

DMAIC Project Road Map

(Note: this slide or the next one is for your use to track progress over project execution and is recommended to be used through project completion and then can be removed from the actual final project ppt before submittal to AAA for certification)



Identify Project CTQ

- Identify Opportunities for Improvement
- Understand Voice of the Customer
- Select Project

Develop Team Charter

- ➔ Define project goals, objectives, scope
- ➔ Form Cross-Functional Team
- ➔ Identify key resources (Black Belt, Master BB, Champion, etc.)
- Begin Building Knowledge notebook

Tollgate

- Update Knowledge Notebook
- Review with Champion, team, etc.
- Formal Project Presentation

Define Process

- ➔ IPO
- ➔ Measurement Plan
- ➔ Fishbone
- ➔ Process Map

Plan for Data Collection

- Collect Data
- Pareto of Opportunities
- Measurement Findings
- Update Financial Benefits form

Validate Measurement System

- ➔ MSA

Establish Process Capability

- ➔ Asses current capability and problem areas

Tollgate

- Update Knowledge Notebook
- Review with Champion, team, etc
- ➔ Formal Project Presentation

Benchmark Analysis

- Determine gap between current performance and goal
- Perform detailed process and data analysis
- Analyze and determine root cause (s) of problems
- ➔ Identify key input variables
- ➔ Discover the relationship between the inputs and outputs

Analyze Data to Discover Relationships

- Quantify Root Causes
- %Variation Explained
- ➔ Screen potential causes
- Verify root causes

Tollgate

- Update Knowledge Notebook
- Review with Champion, team, etc.
- ➔ Formal Project Presentation

Identify Solutions

- ➔ Identify and test proposed solutions
- ➔ Prioritized Potential Solutions
- ➔ Select best solution and predict new capability
- Pilot solution
- ➔ Update process maps, SOPs, etc.

Establish Tolerances / Pilot Solution

- Gather data and validate improvement
- ➔ ROI Analysis
- "To-Be" Process Maps
- ➔ Risk Assessment / FMEA / Contingency Plan
- Establish Tolerances (Xs)

Tollgate

- Update Knowledge Notebook
- Review with Champion, team, etc.
- ➔ Formal Project Presentation

Monitor New Process Capability

- Validate Success (s)
- ➔ Implement Full Solution
- ➔ Final Sigma
- Control Chart
- Graphical and Statistical Analysis

Implement Process Control System & Close Project

- ➔ Control/Response Plan Implemented
- Finalize To-Be Process Maps and Procedures
- ➔ Summarize best practices and lessons learned
- ➔ Celebrate and Communicate Results

Tollgate

- Update Knowledge Notebook
- ➔ Finalize financial benefits
- ➔ Finalize project documentation
- ➔ Final Formal Presentation

